REMARKS/ARGUMENTS

The claims pending in the application are claims 85 - 103, inclusive. All other claims have been cancelled, applicant reserving the right to file one or more divisional applications directed to the nonelected withdrawn claims.

Claims 1 - 15 and 52 - 55 have been rewritten as claims 85 - 103, respectively.

The amendments to the claims clarify that (1) the integrated circuit must contain two or more scan cores and (2) faults to be debugged or diagnosed comprise stuck-type faults and non-stuck-type delay faults.

The rejection of claims 52, 53 and 55 (now claims 102, 103 and 105) being anticipated by Kim (US 6,122,762) is respectfully traversed. Kim does not teach or suggest how to test "two or more" scan cores. The present invention is mainly for debugging or diagnosing two or more scan cores as now clearly defined in the independent claims 85 (formerly claim 1) and 100 (formerly claim 52). In addition, the present invention debugs/diagnoses "at-speed" delay faults, each scan clock must comprise two system clock cycles, whereas to debug/diagnose stuck-type delay faults, each scan clock can comprise only one clock cycle. Thus, applicants' invention uses the term "selected fault type" that allows the DFD circuitry to generate required clock cycles.

Neither Kim nor Rutkowski (US 5,623,503), however, teaches or suggests how to provide such fault type in order for the debug

controller 400 (in the Kim reference) or the partial-scan controller 36 (in the Rutkowski reference) to generate the required clock cycles.

With the advance in deep sub-micron manufacturing, an integrated circuit can now contain 30 to 50 clock domains (or scan cores) each controlled by one scan clock (or system clock). During debug or diagnosis, we can no longer assume that we can test all scan cores simultaneously, because the generated heat and test power could potentially damage the chip. Thus, it is required to provide a DFD selector to indicate which scan cores should be or should not be tested simultaneously.

Therefore, the invention includes the feature recited in Claim 85 reading:

> ...a DFD selector for indicating which said scan cores and said selected fault type will be debugged or diagnosed simultaneously...

which is neither taught nor suggested by the art. Claims 86 - 99 depend from claim 85 and are patentable for the same reasons, *inter alia*.

Likewise, the invention includes the feature in claim 102 directed to the SELECT command for initializing the "DFD selector" and its "selected fault type" given in claim 100, clause (b) reading:

> ...issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores...

is neither taught nor suggested by the prior art. Claims 101 - 103 depend from claim 100 and are patentable for the same reasons.

In view of the above, further and favorable reconsideration is respectfully requested.

Respectfully submitted,

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In the event this paper is deemed not timely filed, the applicant hereby petitions for an appropriate extension of time. The fee for this extension may be charged to Deposit Account No. 26-0090 along with any other additional fees which may be required with respect to this paper.